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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,047	03/31/2004	Li Wei Chu	MR2349-1003	4864

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EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/813,047	CHU ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

(All references are made according to PGPUB # US 2005/0223126 A1 of present application # 10/813047).

In paragraph [0023], lines 5-6, "either 8 bit or 16 bit" should be "either 8-byte or 16-byte".

As per paragraph [0016] of PGPUB, microprocessor detects memory types (i.e. 8-byte or 16-byte) from state register. Paragraph [0023], lines 4-5, it means that value of the state register is set by reading first memory. It is not clear from the descriptions of paragraphs [0016] and [0023], what applicant means, the type of the first memory (i.e. 8-byte or 16-byte) is decided from value of state register as mentioned in paragraph [0016] or the value of state register is set after finding out the memory type as mentioned in paragraph [0023], step (s104). Also from statement (paragraph [0023] and referring to fig.2, step (110)), "reading the state of the first memory and storing the state of the first memory to set the state of the first memory in the state register", it is not clear what is meant, (because according to steps s(104) and s(108), the data type (i.e. 8-byte or 16-byte) is already known and set) setting state register value to detect memory type or reading first memory to set state register?

Appropriate correction is required.

Claim Objections

2. Claim 8 is objected to because of the following informalities: Claim 8, line 11, "a data register used to read a state of the first memory" should be "a state register used to read a state of the first memory". Appropriate correction is required.

3. Acronyms (such as ALEH and ALEL in claim 11) should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim, or in a claim to which it depends. An acceptable correction would be for example in claim 11, Address Latch Enable High (ALEH).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, it is not clear what it meant by "wherein the first memory and the second memory transmit data to each other through the processor". It is not clear from the statement that memories are transmitting data to each other through microprocessor as transmission medium or instructed by the microprocessor.

Claims 2-8 are also rejected due to their dependency on claim 1.

6. Claim 8 recite the limitations "the address data" and "the transmission data" in lines 5 and 9. There is insufficient antecedent basis for these limitations in the claim.

7. Claim 9 recites the limitation "a memory" in line 4. It is not clear from the term "a memory", which memory a claim refers to? A memory from two memories? Or some other memory?

8. Claims 10,11 and 12 recite the limitation "memories" in line 1.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Tallo et al. (US 6,412,055 B2) (Tallo herein after)

As per claim 1, Tallo teaches a buffer controller between memories (fig. 5), comprising:

a microprocessor used to process data transmission for the memories (fig.), item 500);

a first memory connected to the microprocessor (fig.5, item 510); and

a second memory connected to the microprocessor (fig. 5 item 520);

wherein the first memory and the second memory transmit data to each other through the microprocessor (column 3, lines 15-32, taught as (with respect to figs. 1 and 2) processor is capable of transmitting data from different regions of memory and column 5, lines 18-22).

As per claim 7, Tallo teaches a processor is an 8051 chip (column 3, lines 21-22).

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1, 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Pang (US 2003/0084232 A1).

As per claim 1, Pang teaches a buffer controller between memories (fig. 1), comprising:

a microprocessor used to process data transmission for the memories (fig. 1, Chip 2);

a first memory connected to the controller (fig.1, chip 1); and

a second memory connected to the controller (fig. 1, chip 3);

wherein the first memory and the second memory transmit data to each other through the controller (paragraph [0005], taught as microprocessor fetches instructions from flash memory and saves in results in static random access memory (SRAM)).

As per claims 5, 6 and 7, Pang teaches the first memory is a flash memory (fig. 1, item 3), second memory is SRAM (fig. 1, item 4) and the microprocessor is an 8051 chip (fig. 1, item 1, processor is 8031, which is from same family of microcontrollers).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 3, and 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. (US 2004/0049629 A1) (Miura herein after).

As per claim 1, Miura teaches a buffer controller between memories (fig. 1), comprising:

a controller used to process data transmission for the memories (fig. 1, item 1);

a first memory connected to the microprocessor (fig.1, item 3); and

a second memory connected to the microprocessor (fig. 1, item 4);

wherein the first memory and the second memory transmit data to each other through the controller (paragraph [0110]). Miura fails to teach microprocessor. Miura teaches a controller chip which controls data transmission. It would have been obvious to one having ordinary skill in the art at the time of the invention to use microprocessor to control the data transmission between the memories in place of controller taught by

Miura, since microcontroller are widely available and are known to control transmission between memories (see applicant's specification in background of invention section).

As per claim 3, Miura teaches error correction circuit (paragraphs [0073] and [0103]).

As per claims 5-6, Miura teaches a first memory is a flash memory (chip 1); second memory is a static random access memory (chip 3 and paragraph [0005]).

As per claim 7, Miura teaches a controller chip, which performs controlling of data transmission, and it is well known in the art to use 8051 microcontroller as accessing memories.

As per claim 8, Miura teaches controller comprising:

a command register to transmit write command to first memory (Miura teaches sending address signals and command signals, which inherently teaches a command register (paragraph [0070]);

an address register used to control a transmission of the address data to the first memory (Miura teaches sending respective control signals to respective chips to enable and to read/write data to/from respective memories, (paragraphs [0055]-[0061]) and flash memory is comprising those respective registers (paragraph [0232]), inherently teaches setting value for address register to send address data as Miura sends address signals to first memory (paragraph [0070]);

a control register to enable the first memory and control a read/write pulse duration of the first memory (paragraphs [0057]-[0060], Miura teaches a chip enable signal, clock signal, read/write enable signals);

a data register used to control a data type of the transmission type (paragraph [0070], taught as data equivalent to the transfer data size is readout from flash);

a state register to read a state of the first memory (paragraph [0059], taught as ready/busy, write protect signals).

Claims 9-10 are rejected under same rationales as applied to claims 1 and 8 above.

As per claim 11, Miura teaches Address Latch Enable signals (paragraph [0234]).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. (US 2004/0049629 A1) as applied to claim 1 above, and further in view of Harrington (5,471,639).

As per claim 2, Miura teaches all limitations of claim 1 above but fails to teach a direct memory access (DMA) device. Harrington teaches a DMA device used with processor (fig. 1A, item 40). It would have been obvious to one having ordinary skill in the art at the time of the invention to use DMA device as taught by Harrington in the

system of Miura to relieve microprocessor from data transmission duties as well to increase the speed of data transfer (see Harrington column 1, lines 24-30).

As per claim 4, Miura fails to teach multiplexer. Harrington teaches a multiplexer connecting microprocessor and DMA device (fig. 1A, item 44). It would have been obvious to one having ordinary skill in the art at the time of the invention to use multiplexer as taught by Harrington in the system of Miura to provide bus arbitration so microprocessor and DMA device can share same bus (see column 2, lines 7-12).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. as applied to claims 1, 8 and 9 above, and further in view of Miller et al. (US 2005/0050283 A1).

As per claim 12, Miura teaches method of transmitting data from first memory using internal registers of microprocessor as explained with relations to claims 1, 8 and 9 above but fails to teach different widths of flash memory. Miller teaches accessing flash memory using programmable respective register sets of microprocessor and flash memory (figs. 4, 5a and 5b, paragraphs [0037]-[0042]). It would have been obvious to one having ordinary skill in the art to modify Miura's system with the teachings of Miller

to use programmable register sets to use different kinds of flash memory devices (such as 8-byte or 16-byte) (see Miller paragraph [0040]).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kang et al. (US 2002/00180802 A1) teaches transmitting data to/from processor to memory using internal registers.

Wei et al. (US 2003/0156454 A1) teaches transmitting data from flash to SRAM.

Miura et al. (US 6,791,877 B2) teaches transmitting data to/from flash to DRAM using registers of the controller chip.

Odani (US 6,484,270 B1) teaches accessing flash using CPU buses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

4/28/06

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